Xilinx CORE Generator

1. Start Xilinx CORE Generator
    a. **Windows:** Start → Programs → Xilinx ISE 5 → Accessories → CORE Generator
    b. **UNIX:** From shell, type **coregen** (you will have to source mgc.env and Xilinx settings file /vol/xilinx5/settings.csh first)
2. Create a new CORE Generator project
    a. Click the "Create a new project" button
    b. Create a new directory where you want to place the project and enter it's name in the directory box
    c. In Output Options list, keep the default option (Flow Vendor)
    d. Set Target Architecture to Virtex2P and Overwrite Files to True
    e. In Design Entry list, keep the default options (VHDL and ISE)
    f. Click OK
3. Xilinx offers many cores (VHDL files) that are ready to place on its FPGAs. They are grouped according to their types. The list of groups will be displayed on the left side of the CORE Generator window.
4. Generate a core for FFT
    a. Double click Digital Signal Processing
    b. Double click Transforms
    c. Click FFTs
    d. Select **32 Point Parameterisable Complex Fast Fourier Transform**. You can also right click on it and view the data sheet (PDF file) explaining how the CORE works and what it does. Read this document carefully to understand the port names and how to calculate FFT.
    e. Double click the **32 Point Parameterisable Complex Fast Fourier Transform**.
    f. Enter "myfft32" for component name.
    g. Click Generate (ignore warnings)
5. Go to the project directory and you will see some files. The entity for FFT will be in file myfft32.vhd.
    a. Edit the file → Change **XilinxCoreLib.vfft32_v3_0** to **XilinxCoreLib.vfft32_v2_0**.
    b. Compile this to your work directory and you are ready to instantiate it your VHDL file.
        i. Note: The architecture instantiates a component that is defined in pre-compiled file that exists in ModelSim xilinxcorelib library (you can view the library name in the library list when in ModelSim)